REMARKS

Applicants note the Examiner checked box 5 on the Office Action Summary indicating claims 1-22 were allowed. Applicants will proceed as if the Examiner had checked box 6 indicating claims 1-22 were rejected.

In view of the Examiner's earlier restriction requirement, Applicants retain the right to present claims 23-29 in a divisional application.

The Examiner objected to the drawings, stating: "The drawings must show every feature of the invention specified in the claims. Therefore, the functional gate conductors include conductors of at least two different widths (claims 2, and 13) must be shown or the feature(s) canceled from the claim(s). It does not appear that the figures show functional gate conductors with different widths. No new matter should be entered. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application." In response, Applicants point out that Applicants FIG. 5 clearly shows various functional gate conductors 415B having different widths W_T, W_1, W_2 and W_3. Applicants respectfully request the Examiner withdraw his requirement for corrected drawing sheets.

The Examiner rejected claims 1,4-6, 9-12, 15-17 and 20-22 under 35 U.S.C. §102(b) as being unpatentable over U.S. 5,767,542 to Nakamura.

The Examiner rejected claims 1-6, 9, 12-17 and 20 under 35 U.S.C. §102(e) as being unpatentable over U.S. 6,660,462 to Fukuda.

The Examiner rejected claims X-Y under 35 U.S.C. 103(a) as being unpatentable over U.S. 5,767,542 to Nakamura.

Applicants respectfully traverse the §102(b), §102(e) and §103(a) rejections with the following arguments.

35 USC § 102

As to claims 1 and 12, the Examiner states that "Nakamura discloses (see, for example, Fig. 8) an array of field effect transistors (electronic device) comprising a P substrate (semiconductor substrate) 46, dummy gate conductors G2 of MID, GI of M2D; and gate conductors G1 of Ml, G2 of M2. The gate conductors are positioned substantially parallel to each other in a widthwise direction and periodically spaced apart a fixed distance in a direction substantially perpendicular to said widthwise direction 8."

As to claims 1 and 12, the Examiner also states "Fukuda discloses (see, for example, FIG. 11) a semiconductor device (electronic device) comprising a semiconductor substrate, dummy gate patterns (dummy gate conductors) 19, and transistor gate patterns (functional gate conductors) 18. The dummy gate patterns and transistor gate patterns are positioned substantially parallel to each other in a widthwise direction and periodically spaced apart a fixed distance in a direction substantially perpendicular to said widthwise direction."

Applicants contend that claim 1 is not anticipated by Nakamura or Fukuda because Nakamura or Fukuda does not teach each and every feature of claim 1. As a first example Nakamura or Fukuda does not teach "said dummy gates positioned over a gate dielectric layer over a trench filled with an insulating layer formed in said semiconductor substrate" Applicants respectfully point out that Nakamura teaches semiconductor material under the dummy gates and Fukuda has no teaching of a "gate dielectric layer over a trench filled with an insulating layer" under the alleged dummy gates.

As a second example, Nakamura does not teach or suggest "said dummy gate conductors not positioned between adjacent functional gate conductors." Applicants respectfully point out

Nakamura specifically teaches in FIG. 8, dummy gates dispersed between functional gates as the Examiner has pointed out.

As a third example, Nakamura does not teach or suggest "said dummy gate conductors positioned adjacent to ends of said functional gate conductors." Applicants respectfully point out again respectfully point out Nakamura specifically teaches in FIG. 8, dummy gates dispersed between functional gates not "adjacent to ends of said functional gate conductors" as Applicants claim requires.

As a fourth example, Fukuda does not teach or suggest "a transistor in said substrate." Applicants respectfully point out Fukuda teaches and claims only gate patterns and teaches the gate patterns simply on top of a substrate 11 (see Fukuda FIG. 8c).

Based on the preceding arguments, Applicants respectfully maintain that claim 1 is not unpatentable over Nakamura or Fukuda and is in condition for allowance. Since claims 2-11 depend from claim 1, Applicants respectfully maintain that claims 2-11 are likewise in condition for allowance.

Applicants maintain the arguments presented *supra* with respect to claim 1 also apply to claim 12 and Applicants respectfully maintain that claim 12 is not unpatentable over Nakamura or Fukuda and is in condition for allowance. Since claims 13-22 depend from claim 12, Applicants respectfully maintain that claims 13-22 are likewise in condition for allowance.

35 USC § 103 Rejections

As to claims 7, 8, 18 and 19 the Examiner states "Nakamura discloses (see, for example, Fig. 8) an array of field effect transistors (electronic device) comprising a P substrate (semiconductor substrate) 46, dummy gate conductors G2 of M1D, G1 of M2D; and gate conductors G1 of M1, G2 of M2. The gate conductors are positioned substantially parallel to each other in a widthwise direction and periodically spaced apart a fixed distance in a direction substantially perpendicular to said widthwise direction. See paragraph 4, and Fig. 8 above. Nakamura does not disclose the length of said functional gate conductors being a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said fixed distance, and the length of said dummy gate conductors being a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said fixed distance. However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the length of said functional gate conductors and dummy gate conductors in order to match the transistors on a semiconductor substrate and improve a FET circuit's performance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the length of said functional gate conductors being a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said fixed distance, and the length of said dummy gate conductors being a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said fixed distance because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the length of said functional gate conductors and dummy gate conductors in order to

match the transistors on a semiconductor substrate and improve a circuit's performance. See In re Aller, 105 USPQ 233."

Applicants contend that claim 7, as amended, is not obvious in view of Nakamura because Nakamura does not teach or suggest every feature of claim 7. As a first example, Nakamura does not teach or suggest "wherein the gate length of said functional gate conductors is a function of positive integer multiples of a minimum gate length of said functional gate conductors and of positive integer multiples of said fixed distance."

Applicants cite *In re Antonie*, 559 F.2d 618, 619, 195 U.S.P.Q. 6, 8 (C.C.P.A. 1977) which held that varying a variable to optimize a result is obvious only if the prior art has disclosed that the variable is a result effective variable for optimizing the result. In application to claim 7, the Examiner has not provided any evidence from the prior art demonstrating that "it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the length of said functional gate conductors and dummy gate conductors in order to match the transistors on a semiconductor substrate and improve a FET circuit's performance." In fact, it is the gate width that affects performance (e.g. switching speed) while gate length effects current capacity. Further, not only has the Examiner improperly shifted the burden to the Applicant but has leaped from "it is well known to optimize the performance of a semiconductor device by adjusting the length of said functional gate conductors and dummy gate conductors in order to match the transistors on a semiconductor substrate and improve a FET circuit's performance" to the specific "to have the length of said functional gate conductors being a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said fixed distance" without any support whatever.

Based on the preceding arguments, Applicants respectfully maintain that claim 7 is not unpatentable over Nakamura and is in condition for allowance. Applicants maintain that the arguments presented supra with respect to claim 7 also apply to claim 18 and therefore respectfully maintain that claim 18 is likewise in condition for allowance.

Applicants contend that claim 8, as amended, is not obvious in view of Nakamura because Nakamura does not teach or suggest every feature of claim 87. As a first example, Nakamura does not teach or suggest "wherein the gate length of said dummy gate conductors is a function of positive integer multiples of a minimum gate length of said functional gate conductors and of positive integer multiples of said fixed distance."

Applicants again cite *In re Antonie*, 559 F.2d 618, 619, 195 U.S.P.Q. 6, 8 (C.C.P.A. 1977) which held that varying a variable to optimize a result is obvious only if the prior art has disclosed that the variable is a result effective variable for optimizing the result. In application to claim 7, the Examiner has not provided any evidence from the prior art demonstrating that "it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the length of said functional gate conductors and dummy gate conductors in order to match the transistors on a semiconductor substrate and improve a FET circuit's performance." Applicants respectfully repeat it is the gate width that affects performance (e.g. switching speed) while gate length effects current capacity. Further, not only has the Examiner improperly shifted the burden to the Applicant but has leaped from "it is well known to optimize the performance of a semiconductor device by adjusting the length of said functional gate conductors and dummy gate conductors in order to match the transistors on a semiconductor substrate and improve a FET circuit's performance" to the specific "to have the length of said dummy gate conductors being a function of positive integer multiples of a minimum length of

said gate conductors and of positive integer multiples of said fixed distance" without any support whatever.

Second, Applicants fail to understand how the Examiners alleged well known optimization of dummy gate conductors, which by their very nature are not part of a transistor, can have any effect on the performance of a transistor other than taught by Applicants.

Based on the preceding arguments, Applicants respectfully maintain that claim 8 is not unpatentable over Nakamura and is in condition for allowance. Applicants maintain that the arguments presented supra with respect to claim 8 also apply to claim 19 and therefore respectfully maintain that claim 19 is likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0458.

Respectfully submitted,
FOR: Butt et al.

Dated: 05/24/2005

BY: Jack P. Friedman
Jack P. Friedman
Reg. No. 44,688
FOR:
Anthony M. Palagonia
Registration No.: 41,237

3 Lear Jet Lane, Suite 201
Schmeiser, Olsen & Watts
Latham, New York 12110
(518) 220-1850
Agent Direct Dial Number: (802)-899-5460